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June 14, 2004

IFW

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/828,887 04/21/04 |

Yisuo Li et al.

SHALLOW LOW ENERGY ION IMPLANTATION
INTO PAD OXIDE FOR IMPROVING
THRESHOLD VOLTAGE STABILITY

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on June 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

A handwritten signature in black ink, appearing to read "S. B. Ackerman", is written over the date "6/17/04".

U.S. Patent 4,154,626 to Joy et al., "Process of Making Field Effect Transistor Having Improved Threshold Stability by Ion-Implantation," describes a process of making an FET device with improved threshold stability by ion implantation.

U.S. Patent 6,177,333 to Rhodes, "Method for Making a Trench Isolation for Semiconductor Devices," describes a method for making trench isolations in semiconductor devices.

U.S. Patent Application Publication US 2002/0179997 A1 to Goth et al., "Self-Aligned Corner Vt Enhancement with Isolation Channel Stop by Ion Implantation," describes a process of fabricating an FET device using a simultaneous implantation of the well species at the edge of the device and at the bottom of the shallow trench isolation regions.

U.S. Patent Application Publication US 2001/0021545 A1 to Houlihan et al., "Method for Eliminating Transfer Gate Sacrificial Oxide," describes a method for eliminating the transfer gate sacrificial oxide.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

